UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,112	07/29/2003	Junichi Sakamoto	09812.0498-00000	6984

22852 7590 02/24/2006

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
WOODS, ERIC V	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,112	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Eric Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

The objection to claim 5 is withdrawn because applicant has amended to correct it.

The objection to the drawings is withdrawn because of applicant's amendments to correct the drawing errors.

The objection to the specification is withdrawn in view of applicant's correction of those flaws via amendments.

Applicant's arguments filed 23 November 2005 have been fully considered but they are not persuasive.

Specifically, applicant's primary argument hinges on whether or not Negishi teaches: "a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value" in addition to the results of a comparison of said vertices.

Examiner is not arguing that normalizing the coordinate system would inherently produce a judgment value and a negative judgment value.

This rejection was made under 35 USC 103(a), not 35 USC 102. Negishi can be fairly taken to **suggest** that the region falls within a coordinate system that **could** have negative values. Again, this is entirely dependent upon the system, but in a three-dimensional model of a world (e.g. definition of a view volume for clipping purposes), this model is judged from a perspective, and the view volume must be orthonormal to some coordinate set of basis functions. This requires that any view volume centered on

the origin of such an orthonormal coordinate system (e.g. orthogonal, rectangular coordinate system (standard x, y, and z system)) be able to have negative coordinate values. A standard (x, y, z) tuple in a coordinate system can include negative values, and in standard geometries and Euler space does in fact take on such values – any continuous function (and/or) object has at the least the potential to proceed into the negative region. A view volume centered on the origin of a rectangular coordinate system would inherently protrude into and encompass portions of that space having negative coordinate values. The referred-to judgment values are those generated when the view volume is tested to determine whether or not an object is within the view volume. Applicant has additionally **failed** to explicitly redefine the term 'judgment value', which therefore require examiner to take the broadest reasonable interpretation (*In re Morris*, MPEP 2111) of the claims in a manner that is reasonably consistent with the rest of the application. In such case, 'judgment value' can be easily construed to mean a value generated to determine whether or not an object is inside of the view volume.

Also (and more importantly), the clip codes in Negishi have clip **state** codes (see Figure 7), where these could be taken to represent 'judgment reference values' as well as 'negative judgment reference values.' Therefore, Negishi in fact teach the recited limitations under either interpretation.

Examiner is clarifying the record and pointing out that the 'clipin' and 'clipout' functionality does exist, where the object is compared to both flags to generate the clip codes, and the above discussion on view volumes serves as proof that it would have

been obvious to use both positive and negative judgment values as explained in more detail in the rejections below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-2 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi et al (US Patent 6,005,590)('Negishi').

As to claim 1,

A clipping device for judging whether or not ' vertices expressed by a predetermined coordinate system are inside or outside a multi-dimensional region of an object to be drawn, comprising: (preamble ignored as per *In re Hirao* and *Kropa v. Robie*, as it only recites an intended use, and the claimed process steps or apparatus parts can stand by themselves and perform the intended function)

-A clip code generation circuit for generating clip codes obtained by setting data in accordance with results of a comparison of coordinates of said vertices and a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value as bit data; (Negishi in Figure 3 teaches a clip code generating circuit, where FPU (floating point units) 103, 104, and 105 generate clip codes (7:52-8:15) that then are passed to shift registers 304, 305, and 306. As set forth (7:52-8:15) by Negishi, the clip codes are generated by comparing the coordinates of the vertices and the reference values (e.g. X=XMAX and X=XMIN) for comparison through the clipping region (which prima facie is multi-dimensional (see Figures 5-7 and the explanations provided in the cited references, and these are clearly bit data since they are in the memory of a digital computer. It would be obvious, as shown in Figure 6 and further explained in 8:64-10:7, that each vertex is processed on its own, which teaches vertices, and the recited 'judgment values' are merely the bounding coordinates of the clipping region and/or the guardband.)(Negishi also generates clip state codes (see Figure 7, 8:45-65), where these state codes indicate whether an object is inside, outside, or intersects the specific view volume. These codes can be taken to embody positive and negative judgment values as required by the claim, since they indicate where the object is, and specific information with relation to the vertex)

-Clip registers for shifting the clip codes generated at said clip code generation circuit; and (The resulting clip codes from FPU 103, 104, and 105 are then sent to shift registers 304, 305, and 306 which are comparable to applicant's "clip registers". The

results are then passed on to generic clip code register 308. The system works as specified above (8:48-64).)

-A logic circuit for performing a logic operation with respect to all bit data set in said clip registers and setting a clip flag indicating whether or not a vertex to be judged is inside or outside the multi-dimensional region of the object to be drawn. (Element 307, Figure 3, the clip state code generator is clearly "a logic circuit" and it performs operations on the clip codes to generate clip state codes (7:52-8:25). Further, Figure 5(a) provides an example of how that portion of the system works (8:27-47), where the clip state codes indicate whether an object is inside or outside the clip region as explained therein. Further, the fourth embodiment shown in Figure10 has a mask register 1001 that is explicitly taught to perform logical operations against the entire contents of the target register in terms of a comparison operation (see 11:15-60))

Reference Negishi therefore teaches all of the limitations of the instant claim as set forth above except for stating explicitly that the vertex is compared with both the judgment value and a negative judgment value. However, one of ordinary skill in the art would appreciate that the judgment values merely define the bounding region of the two- or three-dimensional region or volume, and that if the coordinate system were normalized so that the zero value and/or origin was situation within the clipping region or volume. One of ordinary skill in the art at the time the invention was made would understand that such a modification would be trivial and could be advantageous since it would reduce the amount of processing necessary to perform the comparisons. In any case, the limitation of negative judgment value is truly irrelevant because the values of

such judgment values is entirely dependent upon the coordinate system used and the bounding region defined by such a system, which may not be symmetric and/or axisymmetric. Therefore, since the system of Negishi generates judgment value results for at least positive vertices, it would be obvious to do so for both upper and lower bounds as tested for by XMIN, XMAX, and the like.

Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second embodiment of Negishi such that it had the mask register in the fourth embodiment, so that the masking and comparison could be performed in such a way that allowed for conditional judgments and jump instructions to be used, which would clearly give it more flexibility.

Additionally, Negishi teaches above the use of clip state codes that are output with the clip codes the constitute the judgment values that are required, where the comparisons are done based on these values and meet the limitations of the instant claim. At the least, such modification to do both comparisons would have been obvious in light of the reference as explained above, since both the min and max are tested against judgment values (e.g. clipin, clipout (in region and out of region)) anyway, where this constitutes the key idea of two tests with respect to the clip codes.

As to claim 2, clearly as shown in Figures 5(a)-5(b) and 6 and as explained above in 7:52-8:16, the system of Negishi utilizes coordinates of vertices in 3-space, that is utilizes a three-dimensional coordinate system, and such vertices therefore correspond to a plurality of coordinate axes. Clearly, as explained in 8:15-10:20 in the example provided for Figures 6 and 7, the clip codes generated by FPUs 103-105,

clearly constitute a 'plurality of clip codes' that do correspond to the coordinate axes. Clearly since such clip codes are then output to shift registers 304-306, the clip registers must inherently have a capacity for holding at least those clip codes, as recited in the cited sections, as discussed in the rejection to the parent claim above, and it would be obvious.

Claims 3-4 are rejected under 35 U.S.C. 103(a) as unpatentable over Negishi as applied to claim 1 above, and further in view of Inoue.

As to claim 3,

A clipping device as set forth in claim 1, wherein said clip code generation circuit generates said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference value.

Reference Negishi does not explicitly teach the use of an absolute value operator, but does teach the setting of a target volume with the area around it, and the checking of a vertex to see if it is in the test volume and within the clip volume and the setting of flags thereof. Reference Inoue teaches the use of absolute values in clipping preprocessing circuits, specifically 2:19-41 teaches that the clipping device performs an operation (subtraction) on the absolute value of a vertex coordinate and a pair of boundaries, wherein similar to Negishi the clip data of the boundaries are put into the register and the check is performed, and the code data recited by applicant clearly is

stored (from the axis basis). Further, Table 1 in Inoue illustrates (1:53-63) how codes are created for the view volume. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuit of Negishi with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Negishi is meant to only accommodate standard (x, y, z) coordinates in the cited embodiment.

As to claim 4,

A clipping device as set forth in claim 2, wherein said clip code generation circuit said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference value.

See the rejection to claim 3 above. The additional limitations of claim 2 are all taught by the primary reference as discussed in the rejection of claim 2. The claim wording is the same with the substitution of only "claim 2" for "claim 1". Therefore, the entirety of that rejection, along with the motivation and combination, is incorporated herein by reference without further comment.

Claim 5 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi et al (US Patent 6,005,590)('Negishi') in view of Koss.

A clipping device for judging whether or not vertices of a primitive expressed by a predetermined coordinate system are inside or outside a multi-dimensional region of an object to be drawn, a polyhedron being drawn in units of primitives including a plurality

of vertices, comprising: (preamble ignored as per *In re Hirao* and *Kropa v. Robie*, as it only recites an intended use, and the claimed process steps or apparatus parts can stand by themselves and perform the intended function. Secondly, the system of Negishi clearly teaches in the abstract that the system is intended to operate in three-dimensions, and the examples shown in Figures 4 and 6 for example show three-dimensional coordinate space, and clearly a three-dimensional object would be composed of triangles or the like, and clearly Negishi teaches as set forth below processing this kind of item, and in Figures 4 and 6 such triangles are shown.)

-A clip code generation circuit for generating clip codes obtained by setting data in accordance with results of a comparison of vertex coordinates of said primitive and a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value as bit data for the amount of the vertexes of the primitive; (Negishi in Figure 3 teaches a clip code generating circuit, where FPU (floating point units) 103, 104, and 105 generate clip codes (7:52-8:15) that then are passed to shift registers 304, 305, and 306. As set forth (7:52-8:15) by Negishi, the clip codes are generated by comparing the coordinates of the vertices and the reference values (e.g. X=XMAX and X=XMIN) for comparison through the clipping region (which prima facie is multi-dimensional (see Figures 5-7 and the explanations provided in the cited references, and these are clearly bit data since they are in the memory of a digital computer. It would be obvious, as shown in Figure 6 and further explained in 8:64-10:7, that each vertex is processed on its own, which teaches vertices, and the recited 'judgment values' are merely the bounding coordinates of the clipping region and/or the

guardband. Further, clearly the examples of Negishi teach that a primitive (e.g. a triangle) is processed by the number of vertices, in this case three, and clearly the embodiment shown in Figure 1 shows that a four-vertex version is used (6:15-56); indeed, in 7:30-48 it states that any number of FPUs can be used to accommodate any number of vertices or the like)

-A current clip register for a shifting the clip codes generated at said clip code generation circuit in accordance with a control signal; (Koss 9:38-51 discloses vertex clip code shift registers, which *prima facie* perform the recited functionality, since clip codes are *prima facie* generated by a clip code generating circuit and, if necessary, moved utilizing the clip code bus disclosed earlier. However, more specifically, Fig. 7 shows a shift register wherein coordinates are shifted in response to a control signal (12:30-60) and discloses how clip codes are shifted in that manner as well)(Inoue teaches registers for this processing in 2:19-41.)

-Clip registers of at least a number smaller than the number of vertexes of said primitive by one cascade connected to an output of said current clip register and able to replace the held data with the clip codes held by the register of a previous stage in accordance with a control signal; (Koss 9:38-51 discloses vertex clip code shift registers, which *prima facie* perform the recited functionality (Fig. 7). Cascade connection is shown in Figure 4 with the elements shown being in horizontal configuration, which would back up the construction shown in Fig. 7, with the cascade construction stated in 9:51-57 because for six one bit cells to be connected together to create a six-bit register, they have to be cascaded. It would be obvious to use cascade connection even though the

word "cascade" is not explicitly used; after all, this is the configuration shown in the drawings.)(Prima facie, shift instructions within the shift register that overwrite other coordinates or flags in that same register act as replacement operations.)

-A control circuit for outputting said control signal to the current clip register when receiving a clip code generation instruction to shift the clip codes generated at said clip code generation circuit and outputting said control signal to a corresponding clip register so as to replace the clip codes between adjacent clip registers including said current clip register when receiving a replacement instruction; (As discussed in the above paragraph, Koss 9:38-51 discusses the operation of such shift registers, which includes moving data as illustrated in Fig. 7 and structurally discussed in 9:51-58 (that is, that fulfills the adjacent shift register limitation (shown in Fig. 7) and the clip register limitation in general). The vertex load control line 224 for shift-registers (234, 236, 238, 240, 242, and 323, Koss Fig. 4) can be driven by the left stack control unit 122 – Koss Fig. 3) (10:1-24). Also, under some circumstances the shift registers can be controlled by the trivial accept and reject circuit shown below the shift registers in Fig. 4. Either the left stack control unit 122 or the accept/reject logic 250 in Fig. 4.)(Prima facie, shift instructions within the shift register that overwrite other coordinates or flags in that same register act as replacement operations.)(Koss Figure 10 a flowchart of steps is shown. As the systems transitions from step 312 to 316 and complete processing a vertex, a flag is generated internally. Further, once step 316 is complete, the system generates results flag for all vertices (step 318). Koss further teaches in 6:31-47 that a replace mode can exist that will substitute one set of color values (object) for another (texture).

Such a replace mode *prima facie* could obviously be applied to coordinates instead of colors (three values (x, y, z) (R, G, B)). Such replacement mode as discussed above would obviously be applied then, or if only one set of registers was being used, would be applied in between steps 312 and 316 in Koss if only one register were being used (and applicant's claim specifically states that it includes situations where only one register would be used).)(The resulting clip codes from FPU 103, 104, and 105 are then sent to shift registers 304, 305, and 306 that are comparable to applicants "clip registers". The results are then passed on to generic clip code register 308. The system works as specified above (8:48-64).)

-A logic circuit for performing a logic operation with respect to all bit data set in said clip registers and setting a clip flag indicating whether or not a vertex to be judged is inside or outside the multi-dimensional region of the object to be drawn. (Element 307, Figure 3, the clip state code generator is clearly "a logic circuit" and it performs operations on the clip codes to generate clip state codes (7:52-8:25). Further, Figure 5(a) provides an example of how that portion of the system works (8:27-47), where the clip state codes indicate whether an object is inside or outside the clip region as explained therein. Further, the fourth embodiment shown in Figure10 has a mask register 1001 that is explicitly taught to perform logical operations against the entire contents of the target register in terms of a comparison operation (see 11:15-60)) (Koss clearly teaches this as the accept/reject logic element 250 in Fig. 4 (10:25-65).)

Reference Negishi teaches most of the above limitations, but does not expressly teach the limitation concerning the current clip register (although implicitly the common

clip register 308 could partially fulfill that purpose, but that is entirely beside the point). Reference Koss teaches the additional limitations as set forth above. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Negishi with Koss because the system of Koss significantly reduces computational load for primitives and other advantages (3:15-55), the Koss reference is analogous art, and can handle polylines (4:20-35), which would allow the Negishi reference to handle N vertices in a way that would be computationally easier than dividing N primitives into N shift registers as per Negishi's suggestion.

However, one of ordinary skill in the art would appreciate that the judgment values merely define the bounding region of the two- or three-dimensional region or volume, and that if the coordinate system were normalized so that the zero value and/or origin was situation within the clipping region or volume. One of ordinary skill in the art at the time the invention was made would understand that such a modification would be trivial and could be advantageous since it would reduce the amount of processing necessary to perform the comparisons. In any case, the limitation of negative judgment value is truly irrelevant because the values of such judgment values is entirely dependent upon the coordinate system used and the bounding region defined by such a system, which may not be symmetric and/or axisymmetric. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second embodiment of Negishi such that it had the mask register in the fourth embodiment, so that the masking and comparison could be performed in such a way

that allowed for conditional judgments and jump instructions to be used, which would clearly give it more flexibility.

As to claim 6,

A clipping device as set forth in claim 5, wherein said control circuit outputs said control signal to a corresponding clip register so as to replace the clip codes along with the vertex processing in accordance with the type of the primitive.

References Koss and Negishi do not explicitly teach this limitation. Reference Inoue teaches in 1:40-67 and 2:1-11 that different amounts of memory (registers) are required for processing each kind of primitive. Koss teaches in 2:21-51 that the vertex processing circuitry can have three separate processing elements and that the circuitry has an enable input, which *prima facie* obviously could be modified such that each of the circuits had a separate enable function (which seems to borne out 10:20-25, where "enabled shift registers" are discussed, which proves that different registers can be disabled / enabled separately). Given that Koss has three units and Inoue teaches that each type of primitive would take one more set of shift registers (e.g. three primitive types – one, two, or three points or vertices requiring 6, 12, or 18 bits respectively), it would be obvious disable or enable registers based on the processing power required (e.g. the size of the primitive to be processed). The type of primitive would be selected during vertex processing and the appropriate shift registers would be enabled or disabled by the control circuit (Koss 10:24-44) as required, which occurs during the initial vertex processing stage. Finally, Inoue has a dimension selection signal that would perform this function (11:25-32). . It would have been obvious to one having

ordinary skill in the art at the time the invention was made to combine the clipping circuit of Negishi with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Negishi is meant to only accommodate standard (x, y, z) coordinates in the cited embodiment, and clearly Inoue further enables faster processing depending on the type of primitive, as stated above.

As to claim 7,

A clipping device as set forth in claim 5, wherein said control circuit generates a vertex ready flag indicating that the vertexes' worth of clip codes of said primitive are ready at the time of the replacement instruction.

Reference Koss does not explicitly teach this limitation, but in Figure 10 a flowchart of steps is shown. As the systems transitions from step 312 to 316 and complete processing a vertex, a flag is generated internally. Further, once step 316 is complete, the system generates results flag for all vertices (step 318). Koss further teaches in 6:31-47 that a replace mode can exist that will substitute one set of color values (object) for another (texture). Such a replace mode *prima facie* could obviously be applied to coordinates instead of colors (three values (x, y, z) (R, G, B)). Inoue 8:9-23 teaches that vertices are updated, that is, overwritten at a particular signal. Such replacement mode as discussed above would obviously be applied then, or if only one set of registers was being used, would be applied in between steps 312 and 316 in Koss if only one register were being used (and applicant's claim specifically states that it includes situations where only one register would be used).) Further, a replacement mode could also be construed as occurring when the register values are shifted to

generate the clip sub-does, as shown in Fig. 7 of Koss. Motivation and combination is incorporated by reference from the rejection to claim 6 above.

As to claim 8,

A clipping device as set forth in claim 6, wherein said control circuit generates a vertex ready flag indicating that the vertexes' worth of clip codes of said primitive are ready at the time of execution of the replacement instruction.

See the rejection for claim 7, this claim is a substantial duplicate with only the words "claim 6" substituted for "claim 5."

As to claim 11,

A clipping device as set forth in claim 5, wherein:

-Said coordinates of said vertexes include values corresponding to a plurality of coordinate axes of a predetermined coordinate system,

-Said clip code generation circuit generates a plurality of clip codes corresponding to the coordinate axes, and

-Said clip registers have capacities for holding at least said plurality of clip codes.

See rejection to claim 2. Claim 11 is an exact duplicate of claim 2, and the only difference is the substitution of the words "claim 5" for "claim 1". The rejection is based only on the primary reference anyway.

As to claim 12,

A clipping device as set forth in claim 5,

-Wherein the clip code generation circuit generates said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the

absolute value of said vertex coordinates; code data of said vertex coordinates, and code data of said judgment reference values.

See rejection to claim 3. Claim 12 is an exact duplicate of claim 3, and the only difference is the substitution of the words "claim 5" for "claim 1". Therefore, the explanation, motivation, and combination are incorporated herein by reference without further comment.

Claims 9-10 are rejected under 35 U.S.C. 103(a) under Negishi in view of Koss and Inoue as applied to claim 5 (and 6) above, and further in view of Oliver et al (US 5,313,610)('Oliver').

As to claim 9,

A clipping device as set forth in claim 5, wherein said control circuit selectively initializes a desired register among a plurality of clip registers including said current clip register under predetermined conditions.

References Negishi, Koss, and Inoue do not explicitly teach this limitation. Reference Oliver teaches (3:58-67) that registers are selected and initialized through a bus, meaning that such registers can be individually selected and initialized. As shown in Oliver Fig. 2, the registers (40_1-40_K) are controlled by control logic 20 over said bus 14. It is well known in the art to initialize a register to prepare it for use in computational purposes or during a reset. Obviously, the control circuit of Oliver could perform the recited limitation of claim 9, since the clipping circuits of Koss and Inoue have multiple registers, including the "current clip register" recited by applicant as established in the rejections to earlier, parent claims. Given that shift operations where registers are

overwritten are taught (e.g. Fig. 7 in Koss) and replace operations are taught (see discussion in the rejection for claim 7, also Inoue 8:9-23 teaches that vertices are updated, that is, overwritten at a particular signal), these would constitute circumstances that would generate "predetermined conditions" as recited by applicant. Given that Oliver teaches a control circuit for memory systems, e.g. register files, and Koss and Inoue have multiple registers that could *prima facie* obviously be embodied as a register file, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clip circuits of Koss and Inoue with the control logic of Oliver to achieve the selective initialization recited by applicant.

As to claim 10,

A clipping device as set forth in claim 6, wherein said control circuit selectively initializes a desired register among a plurality of clip registers including said current clip register under predetermined conditions.

See the rejection for claim 9; the claim is an exact duplicate of claim 9, with the exception that the words "claim 6" were substituted for "claim 5".

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Woods

February 16, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER